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(54) Image distortion correction circuit for use in a display device

Schaltungsanordnung zur Korrektur der Bildverzerrung in einem Anzeigegerät

Circuit de correction de distorsion d'images pour dispositif d'affichage

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Description

The invention relates to a display device as defined in the precharacterizing part of claim 1.

The invention also relates to a correction circuit for use in such a display device.

A display device and a correction circuit of this type are known from EP-A-110282. In this known display device a geometry model is used for the geometry correction, receiving a signal related to the line deflection current at a first input and a field deflection signal generated by the deflection unit at a second input. The geometry model determines the geometry-corrected deflection signals with reference to these input signals. In this known display device a control signal for the modulatable clock generator is determined with reference to the line deflection signal generated by the deflection unit and a signal fed back *via* an output of the geometry model.

In the definition of a video signal (as transmitted) it is assumed that the picture to be displayed is scanned in an orthogonal pattern at a constant rate of the write spot (= the position where the electron beam impinges upon the phosphor layer). Theoretically, the line and field deflection fields are sawtooth-shaped, at 15625 Hz and 50 Hz, respectively. However, a rectangular picture will not be produced due to the shape of the display tube (too flat). The picture will be pincushion-distorted and the horizontal and vertical components of the spot rate will not be constant either. Other causes of the geometry errors are the position of the electron gun/guns (too close to the display screen, or the display screen is "too flat"), the shape of the deflection fields of the line and field deflection coils, the variation of the deflection sensitivity due to a change of the EHT which results in a phenomenon referred to as breathing, and the non-ideal waveforms of the line and field deflection currents. The picture is then displayed in a geometrically distorted form.

The consistency of the spot rate is (always) improved by giving the currents a sinusoidal shape instead of a sawtooth shape, which is referred to as the S correction. However, since the horizontal deflection current has the shape of an attenuated sine, an (asymmetrical) linearity remains to be corrected. Thus, there will always be errors of a higher order which are still to be corrected.

Moreover, the geometry is disturbed because the line frequency of the incoming video signal is varied.

It is not easy to correct geometry errors by adapting the horizontal deflection current. In fact, very high voltages and very large currents occur in the line deflection circuit which produces much energy. Consequently, the current is difficult to influence and the components used are large, hot, expensive and vulnerable.

Another way of geometry correction is to refrain from correcting the deflection current (or currents) and to adapt the video signal instead, so that the correct information is written at the correct position.

Horizontal correction is most necessary and also easiest, because the information is then only to be shifted within one line. This is referred to as clock modulation. Alternatively, a new pixel content could be computed on the basis of the contents of a plurality of adjacent pixels, which is referred to as scan rate conversion.

In the circuit described in the above-mentioned Patent EP-A-0,110,282, a clock modulator is used in which the line deflection signal is applied in an unchanged (uncorrected) form to the line deflection coil. A signal related to the line deflection is applied to the correction circuit. With reference to this signal, with reference to the signal at the output of the (line) deflection unit and with reference to a hardware geometry model, the correction circuit determines a position error signal. This position error signal is applied as an input signal to the clock generator which determines the rate at which the video signal is read from the memory.

A drawback of this known correction circuit is that the geometry correction is carried out by means of an analog mathematical circuit generating two functions of the input signals. This is only possible in display tubes having very simple geometry errors so that this is not a realistic solution.

A further drawback is that the correction circuit in the known display device is inaccurate and expensive, and that the performance of the correction circuit is too much dependent on the elements of the correction circuit.

It is, *inter alia,* an object of the invention to provide a display device and a correction circuit which do not have the above-mentioned drawbacks.

A first aspect of the invention provides a display device as defined in claim 1.

A second aspect of the invention provides a correction circuit for use in a display device as defined in claim 5.

Advantageous embodiments are defined in the dependent claims.

Advantages of the display device according to the invention are, *inter alia* that a plurality of large-signal components (= non-integrable components) is replaced by small-signal components (integrable), which results in a reduction of costs, greater reliability and less power dissipation and requires less space in the display device.

A further advantage of a small-signal solution is that this solution is more flexible because the required correction can be programmed.

An embodiment of the invention as defined in claim 2 has the advantage that the modulatable clock generator is incorporated in the feedback loop, so that it is not necessary to impose strict requirements on the reliability of the characteristics of the modulatable clock generator.

These and other aspects of the invention will be apparent from and elucidated with reference to the embodiments described hereinafter.

In the drawing

Fig. 1 shows an embodiment of a display device according to the invention, and
Fig. 2 shows an embodiment of a display device in greater detail.

Fig. 1 shows a display device W having an input 1 for receiving an input video signal V_{in}. This may be, for example a YUV signal or an RGB signal. The input 1 is then a triple input. A memory 3 is connected to the input 1. The memory stores the (input) video signal under the control of a first clock signal clk1 applied to an input 4.1. Subsequently, the (output) video signal V_{out} is read (after some time) under the control of a second clock signal clk2 applied to an input 4.2 and supplied at an output 5. The memory 3 comprises, for example two line memories, with a video line being written into the one line memory (under the control of the first clock signal) when the previous video line is read from the other line memory (under the control of the second clock signal). Instead of line memories, the memory 3 may alternatively comprise, for example field memories. Video information can be written and read simultaneously by implementing the memory as an asynchronous dual port memory. The output 5 of the memory is coupled to a control electrode 7 of a display tube 9 (three in a colour display tube). The video signal is displayed on a display screen 11 of the display tube. The display tube generates an electron beam/beams at an intensity which is dependent on the video signal V_{out}. As is common practice, this (these) electron beam(s) are deflected by means of (a) line deflection coil(s) L_l and (a) field deflection coil(s) L_r. The line deflection coil and the field deflection coil are coupled to output terminals 13 and 14, respectively, of a deflection unit 15 for receiving a line deflection signal and a field deflection signal at terminals 17 and 19, respectively. The line and field deflection signals may be corrected for EHT variations, but this will not be further explained.

One side of the line deflection coil remote from the terminal 17 is coupled to a measuring resistor R_m. A measuring transformer may alternatively be used instead of a resistor. The junction point of the line deflection coil and the measuring resistor is coupled to an input 21 of a correction circuit 27. The line deflection circuit is shown in greater detail in Fig. 2.

An output terminal 12 of the deflection unit 15 (which output terminal supplies a line deflection current reference signal I_{lref}) is also coupled to a second input 2 of the memory 3. The signal at the input 2 is written into the memory under the control of the first clock signal clk1 and subsequently read under the control of the second clock signal clk2 and supplied at an output 6. This output is connected to a second input 23 of the correction circuit 27. The correction circuit determines and generates a modulated clock signal with reference to the two input signals (at inputs 21 and 23) and supplies this clock signal at an output 25 as the second clock signal clk2 at the input 4.2 of the memory 3. The modulation of the second clock signal then depends on the necessary geometry correction.

In many cases the first clock signal clk1 will be generated by a clock generator which is controlled by a horizontal and a vertical synchronizing signal (not shown in Fig. 1).

The deflection unit 15 will substantially always be controlled by a synchronizing signal (horizontal (line) and vertical (field) synchronizing signal, not shown in Fig. 1, see Fig. 2 for more details).

Fig. 2 shows an embodiment of a display device W in greater detail. Elements denoted by the same reference numerals as in Fig. 1 have corresponding functions.

The input video signal V_{in} is split up in this embodiment into the usual three components R, G and B and the memory now has three inputs 1.R, 1.G and 1.B for receiving the video signal. Similarly as in Fig. 1, the video signal is written under the control of the first clock signal clk1, which clock signal is applied to the input 4.1 of the memory 3.

Under the control of the second clock signal clk2 (from the correction circuit 27) video information V_{out} is read and supplied at three outputs 5.R, 5.G and 5.B, while the video information is displayed on the display tube. These three outputs are connected to three control electrodes 7.R, 7.G and 7.B of the display tube 9.

The display device W not only receives the (input) video signal V_{in} but also a horizontal (line) synchronizing signal Hsync and a vertical (field) synchronizing signal Vsync. These synchronizing signals are applied to the deflection unit 15. The deflection unit comprises a waveform generator 15.1 for generating a line deflection current reference signal I_{lref} under the control of the horizontal synchronizing signal and the vertical synchronizing signal, which reference signal is applied to the input 2 of the memory 3 *via* the output 12 of the deflection unit. A second output of the waveform generator 15.1 supplies a field deflection signal I_r which is applied to the terminal 19 of the field deflection coil L_r *via* the output 14 of the deflection unit 15 and an output amplifier 8. The waveform generator 15.1 may have, for example a facility for determining the ideal horizontal and vertical deflection signals for the display tube 9 used in the display device W, dependent on the type of display tube used. The waveform generator may also ensure, for example a (possibly) required east-west modulation.

The horizontal synchronizing signal Hsync is also applied to a first phase-locked loop 15.2 (PLL, for example, having a large time constant). A second input of the first phase-locked loop receives a signal from the output (of this loop). The output of the first phase-locked loop is also connected to a first input of a second phase-locked loop 15.3 (PLL having a smaller time constant than the first phase-locked loop), which loop has a second input connected to a measuring coil L_m. The meas-

uring coil has its other terminal connected to a ground reference. Instead of the measuring coil L_m the second input of the second phase-locked loop 15.3 may be connected to the primary winding of the transformer T. The output of the second phase-locked loop is coupled to the output 13 of the deflection unit 15 *via* a control circuit 15.4. The output 13 is connected to a line deflection transistor TR. The emitter of the transistor is connected to the ground reference. The collector of the transistor is connected to a primary winding L_p of a transformer T, which primary winding has its other end connected to a voltage source B. The primary winding L_p and the measuring coil L_m are wound, for example on the same core so as to obtain a retrace signal as the second input signal of the second phase-locked loop.

The secondary winding of the transformer T may be used, for example for generating the EHT required for the display tube 9. In an embodiment in which the EHT is generated separately, the transformer will be replaced by a simple coil, as is common practice.

As is usual in a line deflection circuit, a freewheel diode D and a retrace capacitor C_f are connected across the transistor TR. The line deflection coil L_l, a trace capacitor C_s (S correction capacitor) and the measuring resistor R_m are connected in series to the junction point of the collector of the transistor TR and the primary winding L_p, while a terminal of the measuring resistor which is not connected to the trace capacitor is connected to the ground reference.

The line deflection coil L_l may comprise, for example two separate coils and is substantially always connected to the neck of the display tube 9. For the sake of simplicity the line deflection coil is not shown proximate to the display tube in this embodiment.

The junction point of the trace capacitor C_s and the measuring resistor R_m is connected to the input 21 of the correction circuit 27. The input 23 of the correction circuit 27 receives the modulated signal from the output 6 of the memory 3. The inputs 21 and 23 are connected to two inputs of a differential amplifier 27.1, an output of which supplies the amplified difference of the two input signals to a control input of a voltage-controlled oscillator 27.2 (VCO). The output of the voltage-controlled oscillator is connected to the output 25 of the correction circuit, which output supplies the second clock signal clk2 and is connected to the input 4.2 of the memory 3.

The operation of the correction circuit 27 will now be described in greater detail. The horizontal current reference signal I_{ref} generated by the waveform generator 15.1 is subjected to the same delays *etc.* as the incoming video signal V_{in}. If these signals (I_{ref}, I_r and R, G and B) could be directly applied to the display tube, there would be a geometrically perfect picture on the display screen. Instead, the signals (a three-channel video signal R, G and B and the horizontal current reference signal I_{ref}) are applied to the four inputs (1.R, 1.G, 1.B and 2) of the memory (for example, an asynchronous dual port memory). Here they are written at a constant clock (the first clock signal clk1) (for example, synchronized with the synchronizing signals). At the outputs 5.R, 5.G, 5.B and 6 of the memory these four signals are supplied after some time as output video signal V_{out} and as a modulated reference signal. The timing of these signals combined is now dependent on the modulatable read clock frequency (the second clock signal clk2). The output 13 of the deflection unit furnishes a line deflection signal for the line deflection transistor.

In accordance with the present invention the current reference signal distorted (delayed) by the memory and the real deflection current are compared with each other (by a control means or, for example, by a differential amplifier) and the frequency of the read clock (the second clock signal clk2) is corrected by means of, for example a voltage-controlled oscillator (VCO) in such a way that the difference between these two current signals is minimal. The modulated current reference signal and the deflection current will thereby be equal. Since the video signal and the current reference signal are still in conformity with each other as regards timing after they have been processed in the memory, the video signal is now also in conformity with the real deflection current. The picture geometry is then perfect (at least if I_{ref} is perfect).

The quality of the horizontal geometry correction is now independent of the real waveform of the horizontal deflection current. In principle, all circuit elements for the correction of this current may thus be dispensed with.

The phase of the real deflection current with respect to the incoming video signal is optimally adjusted in such a way that, on average, the memory is half filled. Since this phase cannot be influenced rapidly (the line deflection circuit is slow), it is possible to instantaneously deviate therefrom. With a satisfactory control and provided that it is large enough, the memory can also correct these time base errors.

Several modifications are possible. The output clock may also be generated without a voltage-controlled oscillator, for example by a comparator. This comparator supplies a pulse (edge) whenever the difference between the two signals has become too large. The closed control loop can then react maximally fast.

The horizontal current reference signal, which is first locked with the synchronizing signal of the incoming video signal and is generated and subsequently distorted (modulated) *via* the memory (for example, an asynchronous dual port memory) so as to relate it to the read clock of the memory, may alternatively be directly generated from the last-mentioned clock.

Another embodiment of a correction circuit 27 for use in a display device according to the invention is a comparator whose inputs receive the respective line deflection signals and the reference signal delayed in the memory and whose output supplies a clock signal which is applied to the memory. In this circuit this comparator operates as a self-oscillating circuit and generates a clock signal due to the action of the comparator.

In the embodiments described and shown in the Figures, the memory is always shown with two clock inputs. Instead, it is alternatively possible to use a memory having address inputs and to apply the clock signals to the memory *via* counters. It is further irrelevant for the invention whether the memory is either a digital or an analog memory.

It is also possible to choose a random access memory (RAM) instead of (less expensive) sequentially accessible memories (such as delay lines *etc.*).

Instead of modulating the output clock signal (the second clock signal clk2) it is also possible to modulate the input clock (the first clock signal clk1) of the memory or to modulate the two clock signals in opposite senses.

All the signals I_{lref} and I_r have corrections for realising a geometrically perfect picture, including a possible correction for load variations of the EHT, which is a phenomenon referred to as "breathing".

Corrections in connection with deviations in the shape of the line deflection current are automatically realised so that the shape of the line deflection current is no longer relevant. Existing correction elements may optionally be either maintained or removed.

Claims

1. A display device comprising:

   a display tube (11) for displaying video information (Vout),
   a line deflection coil (Ll) and a field deflection coil (Lr),
   a deflection unit (15) having a first output for applying a line deflection current to the line deflection coil (L1) and a second output for applying a field deflection signal (Ir) to the field deflection coil (Lr),
   a memory (3) having an input (1) for receiving and storing input video information (Vin) under the control of a first clock signal (Clk1), and an output (5) for reading the video information (Vout) to be applied to the display tube (11) under the control of a modulatable second clock signal (Clk2),
   a correction circuit (27) for correcting a position error upon display of the video information (Vout) on the display tube (11), with a first input (21) for receiving an input signal related to the line deflection current (I1), and a second input (23), said correction circuit (27) comprising a modulatable clock generator (27.2) for generating the second clock signal (Clk2) and an output for applying said second clock signal (Clk2) to the memory (3), and
   a waveform generator (15.1) adapted to generate a line deflection current reference signal (Ilref), characterized in that
   the memory (3) has a section for storing the line deflection current reference signal (Ilref) under the control of the first clock signal (Clk1) and for reading a modulated line deflection current reference signal being modulated with the second clock signal (Clk2) from the memory (3), said modulated line deflection current reference signal being applied to the second input of the correction circuit (27).

2. A display device as claimed in Claim 1, characterized in that the correction circuit (27) is adapted to apply a control signal to the modulatable clock generator (27.2) in dependence upon the input signal related to the line deflection current (Il) and the modulated line deflection current reference signal.

3. A display device as claimed in Claim 2, characterized in that the correction circuit (27) comprises a differential amplifier (27.1) coupled to receive the input signal related to the line deflection current (Il) and the modulated line deflection current reference signal for applying the control signal to the modulatable clock generator (27.2).

4. A display device as claimed in Claim 1, characterized in that the waveform generator (15.1) is also dapted to generate the field deflection signal (Ir) which is written into the memory (3) under the control of the first clock signal (Clk1) *via* an extra input of the memory (3) and, while being modulated with the second clock signal (clk2), is read from the memory (3) and applied to the field deflection coil (Lr).

Patentansprüche

1. Wiedergabeanordnung mit:

   einer Wiedergaberöhre (11) zur Wiedergabe von Videoinformation (Vout),
   einer Horizontal-Ablenkspule (Ll) und einer Vertikal-Ablenkspule (Lr),
   einer Ablenkeinheit (15) mit einem ersten Ausgang zum Zuführen eines Horizontal-Ablenkstromes zu der Horizontal-Ablenkspule (L1) und einem zweiten Ausgang zum Zuführen eines Vertikal-Ablenksignals (Lr) zu der Vertikal-Ablenkspule (Lr),
   einem Speicher 3) mit einem Eingang (1) zum Empfangen und Speichern von Eingangsvideoinformation (Vin) unter Ansteuerung eines ersten Taktsignals (Clk1), und mit einem Ausgang (5) zum Auslesen der Videoinformation (Vout), die der Weidergaberöhre (11) unter Ansteuerung eines modulierbaren zweiten Taktsignals (Clk2) zugeführt werden soll,

einer Korrekturschaltung (27) zum Korrigieren eines Positionsfehlers bei der Wiedergabe der Videoinformation (Vout) an der Wiedergaberöhre (11), mit einem ersten Eingang (21) zum Empfangen eines Eingangssignals in bezug auf den Horizontal-Ablenkstrom (I1), und einem zweiten Eingang (23), wobei die genannte Korrekturschaltung (27) einen modulierbaren Taktgenerator (27.2) aufweist zum Erzeugen des zweiten Taktsignals (Clk2) und mit einem Ausgang zum Liefern des genannten zweiten Taktsignals (Clk2) zu dem Speicher (3), und einem Wellenformgenerator (15.1) zum Erzeugen eines Horizontal-Ablenkstrombezugssignals (Ilref), dadurch gekennzeichnet, daß der Speicher (3) einen Teil aufweist zum Speichern des Horizontal-Ablenkstrombezugssignals (Ilref) unter Ansteuerung des ersten Taktsignals Clk1) und zum Auslesen eines modulierten Horizontal-Ablenkstrombezugssignals, das mit dem zweiten Taktsignal (Clk2) moduliert ist, aus dem Speicher (3), wobei das genannte modulierte Horizontal-Ablenkstrombezugssignal dem zweiten Eingang der Korrekturschaltung (27) zugeführt wird.

2. Wiedergabeanordnung nach Anspruch 1, dadurch gekennzeichnet, daß die Korrekturschaltung (27) dem modulierbaren Taktgenerator (27.2) ein Steuersignal zuführt, und zwar in Abhängigkeit von dem Eingangssignal in bezug auf den Horizontal-Ablenkstrom (I1) und das modulierte Horizontal-Ablenkstrombezugssignal.

3. Wiedergabeanordnung nach Anspruch 2, dadurch gekennzeichnet, daß die Korrekturschaltung (27) einen Differenzverstärker (27.1) aufweist, der das auf den Horizontal-Ablenkstrom (I1) und das modulierte Horizontal-Ablenkstrombezugssignal bezogene Eingangssignal empfängt zum Zuführen des Steuersignals zu dem modulierbaren Taktgenerator (27.2).

4. Wiedergabeanordnung nach Anspruch 1, dadurch gekennzeichnet, daß der Wellenformgenerator (15.1) ebenfalls das Vertikal-Ablenksignal (Ir) erzeugt, das in den Speicher (3) unter Ansteuerung des ersten Taktsignals (Clk1) über einen zusätzlichen Eingang des Speichers (3) in denselben eingeschrieben wird, indem es mit dem zweiten Taktsignal (Clk2) moduliert ist, aus dem Speicher (3) ausgelesen und der Vertikal-Ablenkspule (Lr) zugeführt wird.

Revendications

1. Dispositif d'affichage comprenant :

un tube image (11) pour afficher des informations vidéo (V_{out});
une bobine de déviation de ligne (Ll) et une bobine de déviation de trame (Lr);
une unité de déviation (15) comportant une première sortie en vue d'appliquer un courant de déviation de ligne à la bobine de déviation de ligne (Ll) et une deuxième sortie en vue d'appliquer un signal de déviation de trame (Ir) à la bobine de déviation de trame (Lr);
une mémoire (3) comportant une entrée (1) en vue de recevoir et stocker des informations vidéo d'entrée (Vin) sous le contrôle d'un premier signal d'horloge (Clk1), et une sortie (5) en vue de lire les informations vidéo (Vout) à appliquer au tube image (11) sous le contrôle d'un deuxième signal d'horloge modulable (Clk2);
un circuit de correction (27) en vue de corriger une erreur de position lors de l'affichage des informations vidéo (Vout) sur le tube d'affichage (11), avec une première entrée (21) pour recevoir un signal d'entrée lié au courant de déviation de ligne (Il), et une deuxième entrée (23), ledit circuit de correction (27) comprenant un générateur d'impulsions d'horloge modulable (27.2) en vue de générer le deuxième signal d'horloge (Clk2) et une sortie en vue d'appliquer ledit deuxième signal d'horloge (Clk2) à la mémoire (3), et
un générateur de forme d'onde (15.1) propre à générer un signal de référence de courant de déviation de ligne (Ilref), caractérisé en ce que la mémoire (3) comporte une section pour stocker le signal de référence de courant de déviation de ligne (Ilref) sous le contrôle du premier signal d'horloge (Clk1) et en vue de lire un signal de référence de courant de déviation de ligne modulé avec le deuxième signal d'horloge (Clk2) de la mémoire (3), ledit signal de référence de courant de déviation de ligne modulé étant appliqué à la deuxième entrée du circuit de correction (27).

2. Dispositif d'affichage suivant la revendication 1, caractérisé en ce que le circuit de correction (27) est propre à appliquer un signal de commande au générateur d'horloge modulable (27.2) en fonction du signal d'entrée lié au courant de déviation de ligne (Il) et au signal de référence de courant de déviation de ligne modulé.

3. Dispositif d'affichage suivant la revendication 2, caractérisé en ce que le circuit de correction (27) comprend un amplificateur différentiel (27.1) couplé pour recevoir le signal d'entrée lié au courant de déviation de ligne (Il) et le signal de référence de courant de déviation de ligne modulé en vue d'appliquer le signal de commande au générateur d'horloge

modulable (27.2).

4. Dispositif d'affichage suivant la revendication 1, caractérisé en ce que le générateur de formes d'onde (15.1) est également propre à générer le signal de déviation de trame (Ir) qui est écrit dans la mémoire (3) sous le contrôle du premier signal d'horloge (Clk1) par le biais d'une entrée supplémentaire de la mémoire (3) et qui, tout en étant modulé avec le deuxième signal d'horloge (Clk2), est lu depuis la mémoire (3) et appliqué à la bobine de déviation de trame (Lr).

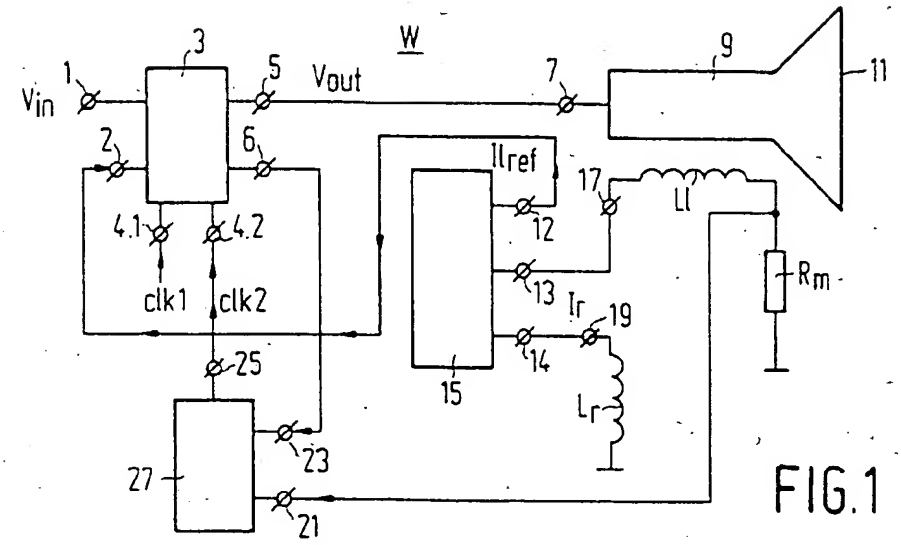
W
Vin
Vout
Ilref
Ir
Ll
Rm
Lr
clk1
clk2

FIG.1

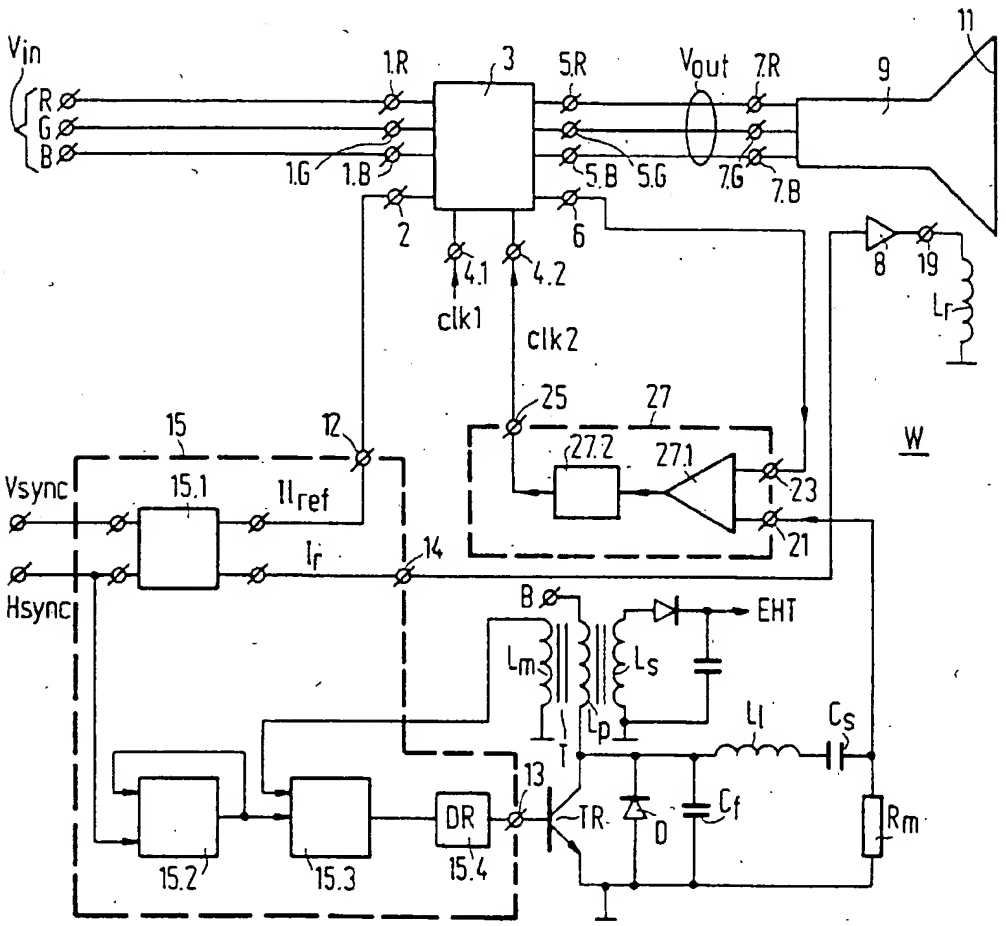
Vin
R
G
B
Vout
W
clk1
clk2
Vsync
Hsync
Ilref
Ir
EHT
Lm
Ls
Lp
Ll
Cs
Cf
TR
D
DR
Rm
Lr

FIG.2